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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/711,673

09/30/2004

Chyh-Yih Chang

13714-US-PA

5672

31561

7590

10/20/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE

7 FLOOR-1, NO. 100

ROOSEVELT ROAD, SECTION 2

TAIPEI, 100

TAIWAN

EXAMINER

MANDALA, VICTOR A

ART UNIT

PAPER NUMBER

2826

DATE MAILED: 10/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/711,673

Applicant(s)

CHANG ET AL

Examiner

Victor A. Mandala Jr.

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 August 2005.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-3, 6-11 and 14-20 is/are rejected.
7) ☒ Claim(s) 4, 5, 12 and 13 is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 6-11, and 14-20 are rejected under 35 U.S.C. 102(e) as being anticipated by

U.S. Patent No. 6,879,003 Cheng et al.

1. Referring to claim 1, a high voltage device for an electrostatic discharge protection device, comprising: a first type epitaxial silicon layer, (Figure 3 #14), disposed in the first type substrate, (Figure 3 #12); a first type well, (Figure 3 #26), disposed in the first type epitaxial silicon layer, (Figure 3 #14); a second type well, (Figure 3 #22), disposed in the first type epitaxial silicon layer, (Figure 3 #14), wherein the second type well, (Figure 3 #22), comprises a second type lightly doped region, (Figure 3 #22), and a second type heavily doped region, (Figure 3 #24), the second type lightly doped region, (Figure 3 #22), is located next to the first type well, (Figure 3 #26), and the second heavily doped region, (Figure 3 #24), is located underneath a portion of the first type well, (Figure 3 #26), and the second type lightly doped region, (Figure 3 #22), wherein the first type well, (Figure 3 #26), adjoins with the second heavily doped region, (Figure 3 #24); a gate structure, (Figure 3 #20), disposed on a portion of the first type well, (Figure 3 #26), and the second type lightly doped region, (Figure 3 #22); a second type first doped region, (Figure 3 #32), and a second type second doped region, (Figure 3

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#34), disposed in the second type lightly doped region, (Figure 3 #22), and the first type well, (Figure 3 #26), on each side of the gate structure, (Figure 3 #20), respectively; a first isolation structure, (Figure 3 #18), disposed in the second type lightly doped region, (Figure 3 #22), and between the gate structure, (Figure 3 #20), and the second type first doped region, (Figure 3 #36); and a first doped region, (Figure 3 #32), disposed in the first type well, (Figure 3 #26), and adjacent to the second type second doped region, (Figure 3 #34).

2. Referring to claim 2, a high voltage device, wherein the second type second lightly doped region, (Figure 3 #22), the first type well, (Figure 3 #26), and the second type second doped region, (Figure 3 #34), together constitute a parasitic bipolar transistor, and the second type heavily doped region, (Figure 3 #24), the first type well, (Figure 3 #26), and the second type second doped region, (Figure 3 #34), together constitute another parasitic bipolar transistor so that a pulse current entering from the second type first doped region, (Figure 3 #32), is able to channel away through the second type second doped region, (Figure 3 #34), after passing through the two parasitic transistors.

3. Referring to claim 3, a high voltage device, wherein the PN junction between the second type heavily doped region, (Figure 3 #24), and the first type well, (Figure 3 #26), has a smaller breakdown voltage than the PN junction between the second type lightly doped region, (Figure 3 #22), and the first well, (Figure 3 #26), and the breakdown voltage of the PN junction between the second heavily doped region, (Figure 3 #24), and the first type well, (Figure 3 #26), is the breakdown voltage of the electrostatic discharge protection circuit.

4. Referring to claim 6, a high voltage device, wherein the first isolation structure comprises a field oxide isolation structure or a shallow trench isolation (STI) structure, (Figure 3 #18).

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5. Referring to claim 7, a high voltage device, wherein the second type first doped region, the second type lightly doped region, (Figure 3 #22), and the second type heavily doped region, (Figure 3 #24), together serves as a drain and the second type second doped region, (Figure 3 #34), serves as a source.

6. Referring to claim 8, a high voltage device, wherein the second type lightly doped region comprises a high voltage second type well, (Figure 3 #36).

7. Referring to claim 9, a high voltage device, wherein the second type heavily doped region comprises a second type buried layer, (Figure 3 #24).

8. Referring to claim 10, a high voltage device, wherein the first type is a P-type and the second type is an N-type, (Figure 3).

9. Referring to claim 11, a high voltage device, comprising: a first type substrate, (Figure 3 #12); a first type epitaxial silicon layer, (Figure 3 #14), disposed in the first type substrate, (Figure 3 #12); a first type well, (Figure 3 #26), disposed in the first type epitaxial silicon layer, (Figure 3 #14); a second type well, (Figure 3 #22), disposed in the first type epitaxial silicon layer, (Figure 3 #14), wherein the second type well, (Figure 3 #22 & 24), comprising a second type lightly doped region, (Figure 3 #22), and a second type heavily doped region, (Figure 3 #24), the second type lightly doped region, (Figure 3 #22), is located next to the second type well, (Figure 3 #22 & 24), and the second heavily doped region, (Figure 3 #24), is located underneath a portion of the first type well, (Figure 3 #26), and the second type lightly doped region, (Figure 3 #22), wherein the first type well, (Figure 3 #26), adjoins with the second heavily doped region, (Figure 3 #24); a gate, (Figure 3 #20), structure disposed on a portion of the first type well, (Figure 3 #26), and the second type lightly doped region, (Figure 3 #22); a

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second type first doped region, (Figure 3 #36), and a second type second doped region, (Figure 3 #34), disposed in the second type lightly doped region, (Figure 3 #22), and the first type well, (Figure 3 #26), on each side of the gate, (Figure 3 #20), structure respectively; a first isolation structure, (Figure 3 #18), disposed in the second type lightly doped region, (Figure 3 #22), and between the gate structure, (Figure 3 #20), and the second type first doped region, (Figure 3 #36); and a first type doped region, (Figure 3 #32), disposed in the first type well, (Figure 3 #26), and adjacent to the second type second doped region, (Figure 3 #34).

10. Referring to claim 14, a high voltage device, wherein the first isolation structure comprises a field oxide isolation structure or a shallow trench (STI) structure, (Figure 3 #18).

11. Referring to claim 15, a high voltage device, wherein the high voltage has a variety of applications in the design of circuits, (Figure 3).

12. Referring to claim 16, a high voltage device, wherein the high voltage device is used inside display driver ICs, power supplies, power administrators, telecommunications, automobile electronics, and industrial controls, (it is inherent that the ESD protection circuit could be used in various application, which would be connected to input output pins of a circuit Col. 1 Lines 39-40).

13. Referring to claim 17, a high voltage device, wherein the second type first doped region, the second type lightly doped region, (Figure 3 #22), and the second type heavily doped region, (Figure 3 #24), together serves as a drain and the second type second doped region, (Figure 3 #34), serves as a source.

14. Referring to claim 18, a high voltage device, wherein the second type lightly doped region comprises a high voltage second type well, (Figure 3 #36).

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15. Referring to claim 19, a high voltage device, wherein the second type heavily doped region comprises a second type buried layer, (Figure 3 #24).

16. Referring to claim 20, a high voltage device, wherein the first type is a P-type and the second type is an N-type, (Figure 3).

Allowable Subject Matter

17. Claims 4 5, 12, and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A. Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


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10/17/05